IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/045,137	Confirmation No.:	3416
First Named Inventor:	Wang, Albert Z. H.	Filing Date:	23 October 2001
Group Art Unit:	2811	Examiner:	Hu, S.
Atty. Docket No.:	NS-3868-2C US		
Title:	Dual Direction Over-Voltage And Over-Current IC Protection Device And Its Cell Structure		
Assignee(s):	National Semiconductor Corporation		

Mountain View, California
19 December 2003

MAIL STOP NON-FEE AMENDMENT
COMMISSIONER FOR PATENTS
PO Box 1450
Alexandria, Virginia 22313-1450

AMENDMENT TO DRAWINGS

Sir:

Responsive to the Office Action mailed 24 September 2003, the drawings for the above patent application should be amended in the following manner.

In Fig. 1A, "P-Sub" should be changed to "P-Substrate".

In Fig. 1B, a dot should be added at each location where one conductor line intersects another conductor line; and a small circle should be added at the top of the top vertical line.

In Fig. 1C, the right-hand portion of the horizontal axis should be shortened; and the label "Voltage" should be moved upward to be horizontally in line with the horizontal axis just beyond the right-hand end of the horizontal axis.

In Fig. 1D, "p-type sub" should be changed to "P-Type Substrate"; and "36", each occurrence, should be changed to "40".

In Fig. 2, "N", each occurrence, should be changed to "n"; and "P", each occurrence, should be changed to "p".

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

In Fig. 3, "N^+", each occurrence, should be changed to "n^+".

In Fig. 4, a dot should be added at each location where one conductor line intersects another conductor line; the two horizontal line segments extending beyond the top horizontal line segment that extends between the two adjoining vertical lines should be deleted; and the hollow arrowhead for transistor 130 should be changed to a solid arrowhead.

In Fig. 5, a dot should be added at each location where one conductor line intersects another conductor line to the extent that such a dot is not already present; the label "P-Base" should be added to each of regions 114 and 118; and a hollow arrowhead pointed toward the upper right should be added to the left-hand slanted line of transistor 140.

In Fig. 6, "I_H" should be changed to "I_h"; "I_T", each occurrence, should be changed to "I_t"; and "V_T", each occurrence, should be changed to "V_t".

In Fig. 7, "N^+", each occurrence, should be changed to "n^+"; "126", each occurrence, should be changed to "146"; and "130", each occurrence, should be changed to "148".

In Fig. 8A, "n-well" should be changed to "N-Well"; slanted shading extending from lower left to upper right should be added to region 116; dotted shading should be added to region 120; and "130" and "132" should be respectively changed to "152" and "154".

In Fig. 9A, the label "N-Well" should be added to region 116; a line should extend from label 114 to the rectangle lying between rectangles 124 and 120; and "130", "132", "134", and "136" should be respectively changed to "162", "164", "166", and "168".

In Fig. 10A, "P-base" should be changed to "P-Base"; the label "N-Well" should be added to region 116; and "130" and "132" should be respectively changed to "172" and "174".

In Fig. 11A, "130", each occurrence, should be changed to "178".

In Fig. 11B, "130", each occurrence, should be changed to "178".

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

In Fig. 12, the label "130" should be added to right-hand transistor; a solid arrowhead pointing toward the upper left should be added to the upper slanted line of newly labeled transistor "130"; a solid arrowhead pointing to the upper left should be added to the right-hand slanted line of transistor 140; a hollow arrowhead pointing to the upper right should be added to the left-hand slanted line of transistor 140; the horizontal line situated directly above transistor 140 should be extended to the right to contact the nearest vertical line; the portion

of the just-mentioned vertical line situated below the just-mentioned horizontal line should be deleted; a dot should be added at each location where one conductor line intersects another conductor line; the label "136" below region 124 should be changed to "138"; labels "116" and "118" should be moved above the horizontal line below which they now lie; and the labels "112", "122", and "114" should be respectively added to the "n^+", "p^+", and "P-Base" regions respectively labeled as regions "112", "122", and "114" in Fig. 3.

In Fig. 13, a solid arrowhead pointing toward the upper left should be added to the upper slanted line of transistor 130; a solid arrowhead pointing toward the lower left should be added to the lower slanted line of transistor 150; a solid arrowhead pointing toward the lower left should be added to upper slanted line of transistor 140; a hollow arrowhead pointing toward the upper left should be added to the lower slanted line of transistor 140; and a dot should be added at each location where one conductor line intersects another conductor line to the extent that such a dot is not already present.

In Fig. 14, a solid arrowhead pointing toward the upper left should be added to the upper slanted line of transistor 130; the arrowhead for transistor 150 should be converted into a solid arrowhead; a solid arrowhead pointing toward the lower left should be added to the upper slanted line of transistor 140; a hollow arrowhead pointing toward the upper left should be added to the lower slanted line of transistor 140; and a dot should be added at each location where one conductor line intersects another conductor line to the extent that such a dot is not already present.

Enclosed are copies of the relevant drawing sheets in which the foregoing changes are indicated in red.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779